UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/824,329	04/14/2004	Yeshwanth Narendar	1035-E4371	5396

34456 7590 03/26/2009

LARSON NEWMAN ABEL & POLANSKY, LLP
5914 WEST COURTYARD DRIVE
SUITE 200
AUSTIN, TX 78730

EXAMINER	
MALDONADO, JULIO J	
ART UNIT	PAPER NUMBER
2823	

MAIL DATE	DELIVERY MODE
03/26/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/824,329	NARENDAR ET AL.	
	Examiner	Art Unit	
	JULIO J. MALDONADO	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-10 and 14-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 5-10, 14-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 2-4, 11-13, and 22-53 as set forth in the reply filed on 12/29/2008 is acknowledged.

2. Claims 1, 5-10, 14-21 are pending in the application.

Claim Objections

3. Claim 1 is objected to because of the following informalities: in claim 1, line 4, where the applicants recite, "...a layer consisting essential...", replace with --a layer consisting essentially--. Appropriate correction is required.

4. Claim 20 is objected to because of the following informalities: in claim 20, line , where the applicants recite, "...a layer consisting essential...", replace with --a layer consisting essentially--. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 5, 6, 8, 9, 14-19 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Thilderkvist et al. (U.S. 6,277,194 B1, hereinafter Thilderkvist) in view of Kumar (U.S. 2003/0198749 A1).

In reference to claims 1, 4-6, 14 and 19, Thilderkvist teaches a semiconductor processing component comprising silicon carbide (SiC), wherein an outer surface of said component consist of a coated layer of SiC, and wherein said coated layer is treated to reduce the amount of contaminants thereon and therein said SiC layer, and wherein said SiC component is a SiC reaction chamber component, a susceptor, wafer lift pins, or any other surfaces that will be in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11).

Thilderkvist fails to disclose wherein said coated SiC is a CVD-SiC.

However, Kumar teaches a semiconductor processing component comprising a coated CVD-SiC on a substrate comprising silicon carbide impregnated with silicon, sintered SiC, wherein an outer surface portion of the component consists essentially of CVD-SiC and wherein said CVD-SiC is clean (Kumar, [0009], [0023] and [0030]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Thilderkvist and Kumar to enable the SiC component according to the teachings of Kumar because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness. See MPEP 2144.07.

The combined teachings of Thilderkvist and Kumar disclose wherein said SiC is a treated SiC to a desired level of purity (Thilderkvist, column 5, lines 12 – 18), but fail to expressly disclose wherein said CVD-SiC has a surface impurity level that is not greater than two times a bulk impurity level when the bulk impurity level is measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

However, the selection of the claimed impurity concentration is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a CVD-SiC with a desired level of purity, and furthermore because both, Thilderkvist and Kumar are directed to a semiconductor component having reduced impurity levels. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the combined teachings of Thilderkvist and Kumar to arrive at the claimed invention.

In reference to claims 8 and 9, the combined teachings of Thilderkvist and Kumar substantially teach all aspects of the invention but fail to expressly disclose wherein the CVD-SiC layer has a thickness within a range of about 10 to about 1,000 μm, and wherein the CVD-SiC layer has a thickness within a range of about 10 to 1000 μm.

However, one of ordinary skill in the art would have been led to the recited dimensions through routine experimentation and optimization to obtain a desired coated semiconductor component. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical, and it appears prima facie that the process would possess utility using another dimension (page 10, [0035] – page 11, [0036]). Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ

232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966). See also MPEP 2144.04(IV)(B).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the combined teachings of Thilderkvist and Kumar to arrive at the claimed invention.

In reference to claims 15-18, the combined teachings of Thilderkvist and Kumar teach wherein contaminants within the semiconductor components include iron (Fe), copper (Cu) and nickel (Ni), for example (Thilderkvist, column 2, lines 31 – 45), but fail to disclose wherein the bulk impurity level is not greater than $1x10^{17}$ atoms/ccFe and not greater than $1x10^{15}$ atoms/ccCr. However, the selection of the impurity level range is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a desired cleaned SiC surface, and furthermore, because Thilderkvist and Kumar are directed to a semiconductor component having reduced metal impurity levels on its surface. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Thilderkvist in view of Kumar to arrive at the claimed invention.

In reference to claim 21, the combined teachings of Thilderkvist and Kumar dislcose wherein the component is machined in an early stage of the manufacturing process (Kumar, [0029]).

The combination of Thilderkvist and Kumar fail to expressly disclose wherein the component is machined prior to treatment to provide said surface impurity level.

However, a "product by process" claim is directed to the product per se, no matter how said product was made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. In re Brown, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); In re Pilkington, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); Buono v. Yankee Maid Dress Corp., 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935). Note that Applicant has burden of proof in such cases as the above case law makes clear.

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thilderkvist ('194) in view of Kumar ('749) as applied to claims 1, 4-6, 8, 9, 14-19 and 21 above, and further in view of Buckley et al. (U.S. 6,488,497 B1, hereinafter Buckley).

The combined teachings of Thilderkvist and Kumar disclose wherein said SiC component is a SiC reaction chamber component, a susceptor, wafer lift pins, or any other surfaces that will be in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11).

The combination of Thilderkvist and Kumar fail to dislcose wherien the substrate comprises recrystallized SiC impregnated with elemental silicon.

However, Buckley discloses wafer boats used for the manufacture of semiconductor components, wherein said wafer boats are conventionally made of recrystallized SiC impregnated with elemental silicon (Buckley, column 2, lines 40 - 53).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Thilderkvist and Kumar to enable the component of Thilderkvist and Kumar according to the teachings of Buckley because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable components in Thilderkvist and Kumar and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07) and because the combination of Thilderkvist and Kumar are open to components having surfaces in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11). The "Fact that claimed combination of elements was "obvious to try" might show that such combination was obvious under 35 U.S.C. §103, since, if there is design need or market pressure to solve problem, and there are finite number of identified, predictable solutions, person of ordinary skill in art has good reason to pursue known options within his or her technical grasp, and if this leads to anticipated success, it is likely product of ordinary skill and common sense, not innovation". 82 USPQ2d 1385 KSR International Co. v. Teleflex Inc.

Therefore, the combined teachings of Thilderkvist, Kumar and Buckley disclose a substrate comprising recrystallized SiC impregnated with elemental silicon.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thilderkvist ('194) in view of Kumar ('749) and Bosch (U.S. 6,890,861 B1).

Thilderkvist teaches a semiconductor processing component comprising silicon carbide (SiC), wherein an outer surface of said component consist of a coated layer of SiC, and wherein said coated layer is treated to reduce the amount of contaminants thereon and therein said SiC layer, and wherein said SiC component is a SiC reaction chamber component, a susceptor, wafer lift pins, or any other surfaces that will be in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11).

Thilderkvist fails to disclose wherein said coated SiC is a CVD-SiC.

However, Kumar teaches a semiconductor processing component comprising a coated CVD-SiC on a substrate comprising silicon carbide impregnated with silicon, sintered SiC, wherein an outer surface portion of the component consists essentially of CVD-SiC and wherein said CVD-SiC is clean (Kumar, [0009], [0023] and [0030]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Thilderkvist and Kumar to enable the SiC component according to the teachings of Kumar because the selection of a known material based on its suitability for its intended use supported a prima facie obviousness. See MPEP 2144.07.

The combined teachings of Thilderkvist and Kumar disclose wherein said SiC is a treated SiC to a desired level of purity (Thilderkvist, column 5, lines 12 – 18), but fail to expressly disclose wherein said CVD-SiC has a surface impurity level that is not greater

than two times a bulk impurity level when the bulk impurity level is measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

However, the selection of the claimed impurity concentration is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a CVD-SiC with a desired level of purity, and furthermore because both, Thilderkvist and Kumar are directed to a semiconductor component having reduced impurity levels. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the combined teachings of Thilderkvist and Kumar to arrive at the claimed invention.

The combined teachings of Thilderkvist and Kumar substantially teach all aspects of the invention including forming the semiconductor component using a sintering process (Kumar, [0009], [0023] and [0030]), but fail to disclose wherein said components are formed by a CVD process.

However, Bosch teaches silicon carbide components or silicon carbide/silicon components such as liners, process tubes, paddles and boats, formed by either sintering and/or CVD processes (Bosch, column 3, lines 32 – 38).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Thilderkvist and Kumar to enable the components of Thilderkvist and Kumar to be formed according to the teachings of Bosch because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable methods of forming the disclosed components of Thilderkvist and

Kumar and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP 2144.07.

9. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thilderkvist ('194) in view of Kumar ('749) and Goldstein et al. (U.S. 5,494,439, hereinafter Goldstein).

Thilderkvist teaches a semiconductor processing component comprising silicon carbide (SiC), wherein an outer surface of said component consist of a coated layer of SiC, and wherein said coated layer is treated to reduce the amount of contaminants thereon and therein said SiC layer, and wherein said SiC component is a SiC reaction chamber component, a susceptor, wafer lift pins, or any other surfaces that will be in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11).

Thilderkvist fails to disclose wherein said coated SiC is a CVD-SiC.

However, Kumar teaches a semiconductor processing component comprising a coated CVD-SiC on a substrate comprising silicon impregnated, sintered SiC, wherein an outer surface portion of the component consists essentially of CVD-SiC and wherein said CVD-SiC is clean (Kumar, [0009], [0023] and [0030]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Thilderkvist and Kumar to enable the SiC component according to the teachings of Kumar because the selection

of a known material based on its suitability for its intended use supported a prima facie obviousness. See MPEP 2144.07.

The combined teachings of Thilderkvist and Kumar disclose wherein said SiC is a treated SiC to a desired level of purity (Thilderkvist, column 5, lines 12 – 18), but fail to expressly disclose wherein said CVD-SiC has a surface impurity level that is not greater than two times a bulk impurity level when the bulk impurity level is measured at a depth of at least 3 μm from an outer surface of the outer surface portion.

However, the selection of the claimed impurity concentration is obvious because it is a matter of determining optimum process condition by routine experimentation with a limited number of species to obtain a CVD-SiC with a desired level of purity, and furthermore because both, Thilderkvist and Kumar are directed to a semiconductor component having reduced impurity levels. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the combined teachings of Thilderkvist and Kumar to arrive at the claimed invention.

The combined teachings of Thilderkvist and Kumar substantially teach all aspects of the invention but fail to disclose wherein the SiC component comprises a wafer boat.

However, Goldstein (Figs.1-3) teaches a semiconductor processing component comprising an ultraclean SiC surface, wherein said outer surface portion of the component is free from metal impurities, wherein said surface is cleaner than an interior bulk of said semiconductor component, and wherein said metal impurities comprise aluminum, sodium and iron (Goldstein, column 2, line 47 – column 8, line 7), and

wherein said component may include boats, cantilevers, tubes, liners, pedestals and pins (Goldstein, column 3, lines 2 – 4).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Thilderkvist and Kumar to enable the components of Thilderkvist and Kumar according to the teachings of Goldstein because one of ordinary skill in the art at the time the invention was made would have been motivated to look to alternative suitable components in Thilderkvist and Kumar and art recognized suitability for an intended purpose has been recognized to be motivation to combine (MPEP 2144.07) and because the combination of Thilderkvist and Kumar are open to components having surfaces in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11). The "Fact that claimed combination of elements was "obvious to try" might show that such combination was obvious under 35 U.S.C. §103, since, if there is design need or market pressure to solve problem, and there are finite number of identified, predictable solutions, person of ordinary skill in art has good reason to pursue known options within his or her technical grasp, and if this leads to anticipated success, it is likely product of ordinary skill and common sense, not innovation". 82 USPQ2d 1385 KSR International Co. v. Teleflex Inc.

Response to Arguments

10. Applicant's arguments filed 12/29/2008 have been fully considered but they are not persuasive.

Applicants argue, "…Applicants respectfully submit that one of ordinary skill in the art would not have modified Thilderkvist to use the same material for the sacrificial layer and the underlying susceptor in view of the repeated coating and removal of the sacrificial layers. If Thilderkvist would be modified such that the underlying susceptor and sacrificial layer to both include SiC, the removal of a sacrificial layer would also remove a portion of the underlying susceptor. Even if the susceptor includes SiC impregnated with elemental Si, one of ordinary skill in the art would have expected the SiC in the underlying susceptor to have been etched and leave the elemental Si and gaps (where SiC was previously present) along the outermost surface of the susceptor. Because one of ordinary skill in the art would have expected the SiC to provide substantially mechanical support, removing the SiC would have substantially degraded the mechanical integrity of the semiconductor processing component. Thus, the modification does not have a reasonable expectation of success. M.P.E.P. § 2143.02…".

In response to the applicants' arguments, the claimed invention is directed to a device and not to a particular procedure to arrive at the claimed device. Thilderkvist discloses a device having silicon carbon coated surface, wherien said coated surface is a treated surface with reduced number of contaminants, wherein said device is a SiC component, and wherein said SiC component is a SiC reaction chamber component, a susceptor, wafer lift pins, or any other surfaces that will be in either direct or close contact with the wafer during process, for example (Thilderkvist, column 3, line 41 – column 5, line 11). Furthermore, Kumar teaches a semiconductor processing

component comprising a coated CVD-SiC on a substrate comprising silicon impregnated, sintered SiC, wherein an outer surface portion of the component consists essentially of CVD-SiC and wherein said CVD-SiC is clean (Kumar, [0009], [0023] and [0030]). Accordingly, the claimed invention is obvious over the teachings of Thilderkvist and Kumar.

Applicants argue, "…Kumar teaches away from semiconductor processing components that are sintered SiC, whether by itself or coated with CVD SiC. More particularly, silicon carbide presents substantial fabrication problems for the complex parts required of plasma reactors. Silicon carbide is one of the hardest commonly found materials and is thus difficult to machine…". In response to the applicants' arguments, Kumar was relied upon devices made of SiC, not on any particular process of manufacture.

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIO J. MALDONADO whose telephone number is (571)272-1864. The examiner can normally be reached on Mon-Fri, 8:00 A.M.-4:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/George Fourson/
Primary Examiner, Art Unit 2823

/J. J. M./
Examiner, Art Unit 2823